

FIG. 1.

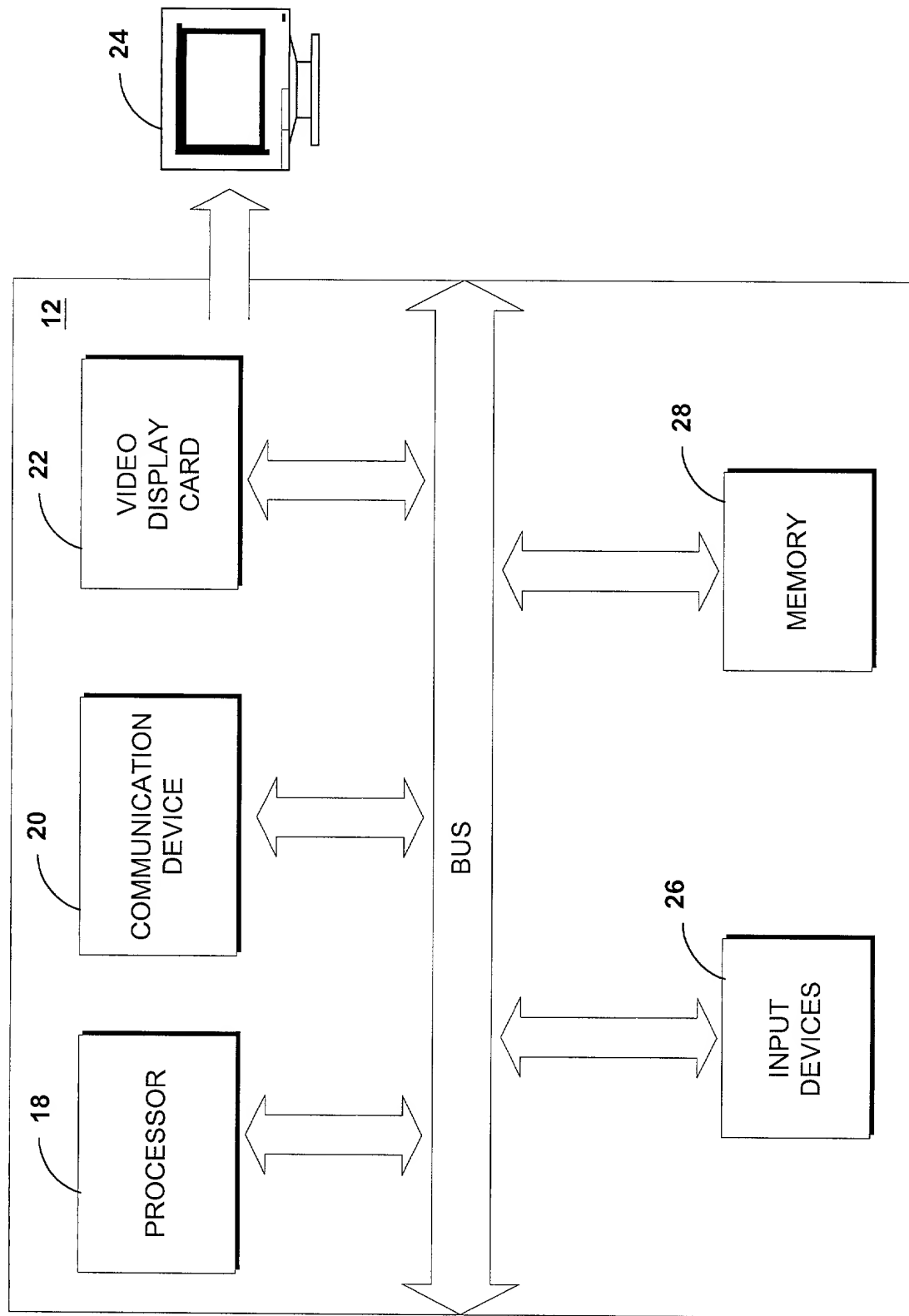


FIG. 2.

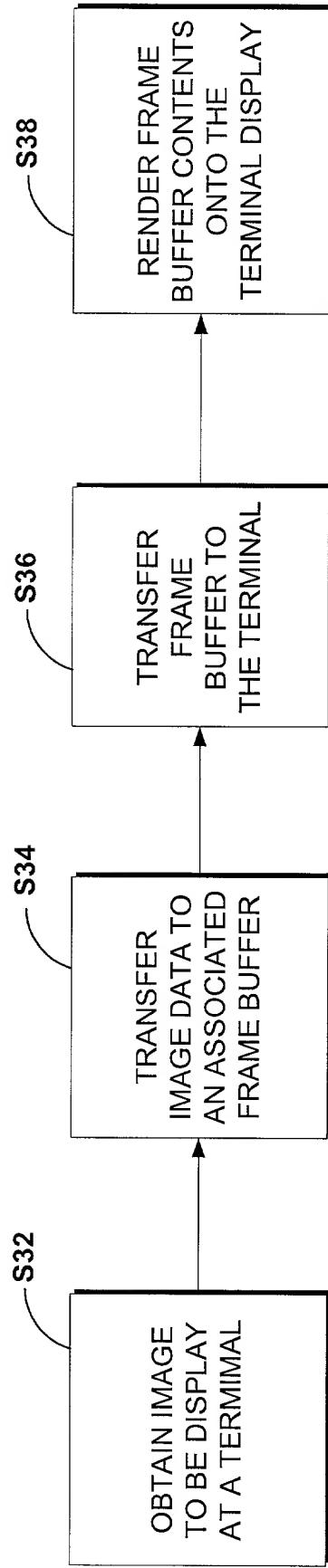


FIG. 3.

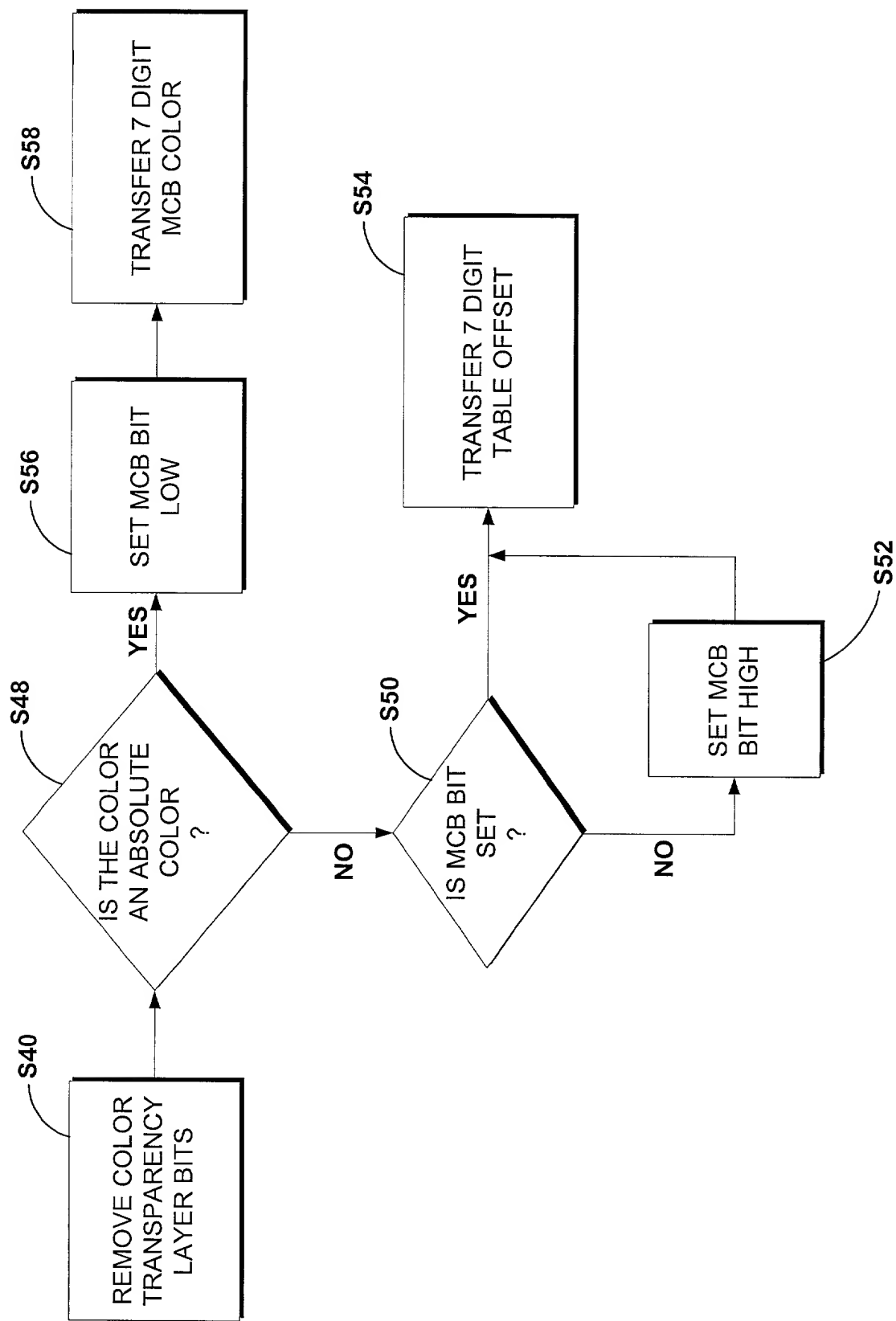


FIG. 4.

FIG. 5 is a block diagram of a system 40 for processing data. The system 40 includes a processor 42, a memory 44, and a data source 46. The processor 42 is connected to the memory 44 and the data source 46. The processor 42 is configured to receive data from the data source 46, process the data, and store the processed data in the memory 44. The memory 44 is configured to store the processed data. The data source 46 is configured to provide data to the processor 42.

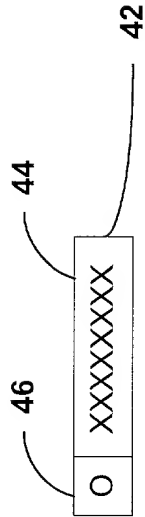


FIG. 5.

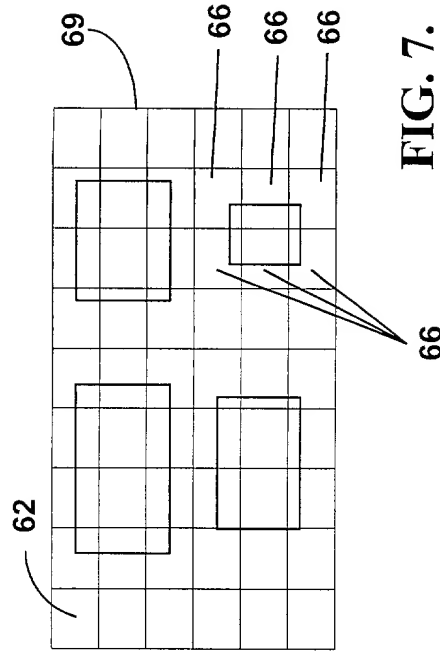
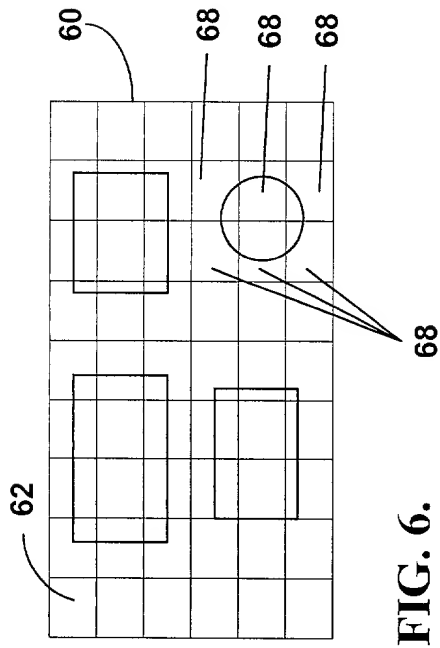


FIG. 8.

AB	CD	EF	GH	IJ	KL	MN	OP	QR
ST	UV	WX	YZ	12	34	56	78	90
00	01	02	03	04	05	06	07	08
09	10	11	12	13	14	15	16	17
18	19	20	21	22	23	24	25	26
27	28	29	30	31	32	33	34	35

FIG. 9.

AB	CD	EF	GH	IJ	KL	MN	OP	QQ
ST	UV	WX	YZ	11	34	56	78	90
00	01	02	03	04	05	06	07	08
09	10	11	12	13	14	15	16	18
18	19	20	21	22	23	24	25	26
27	28	33	30	31	32	33	34	35

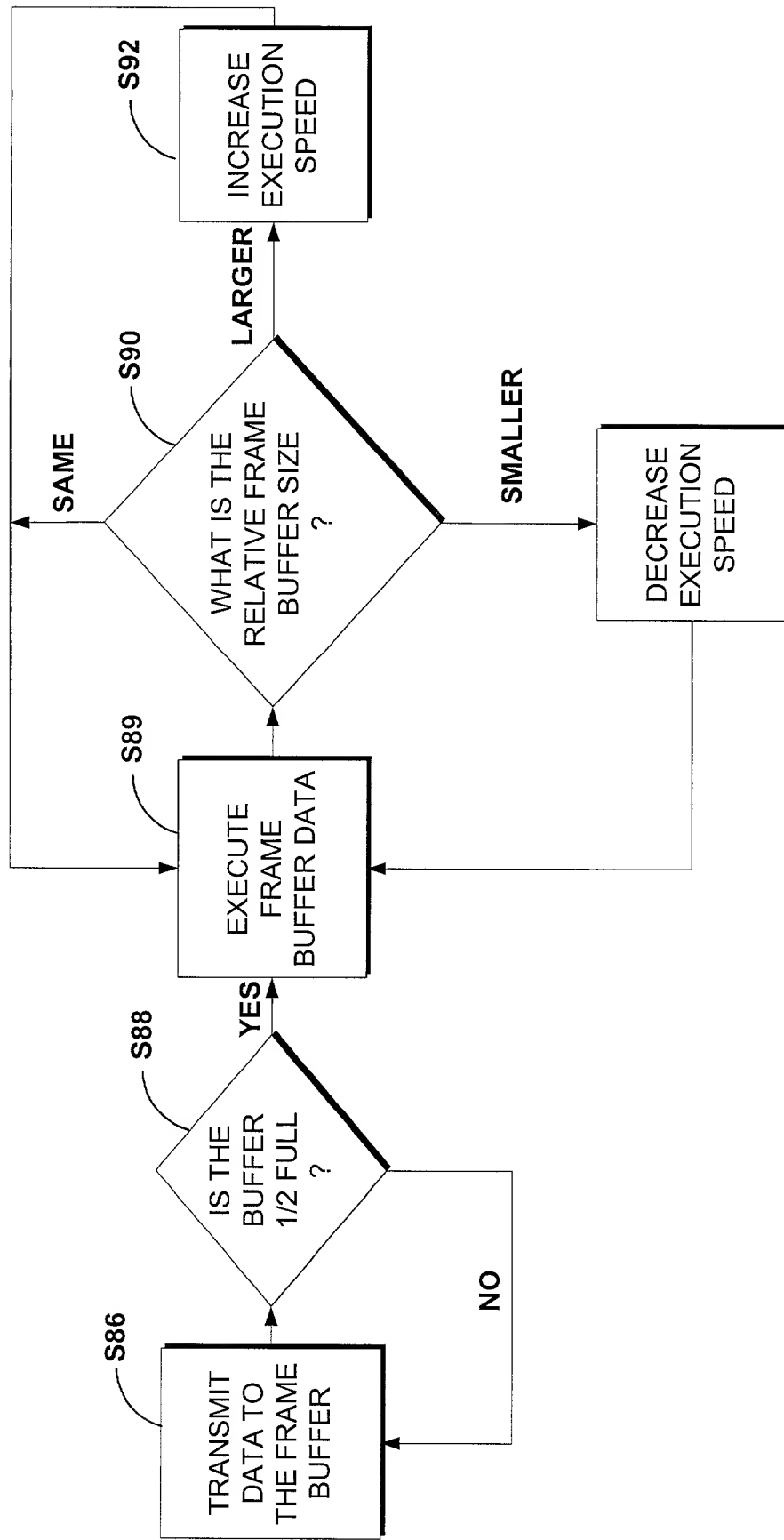


FIG. 10.

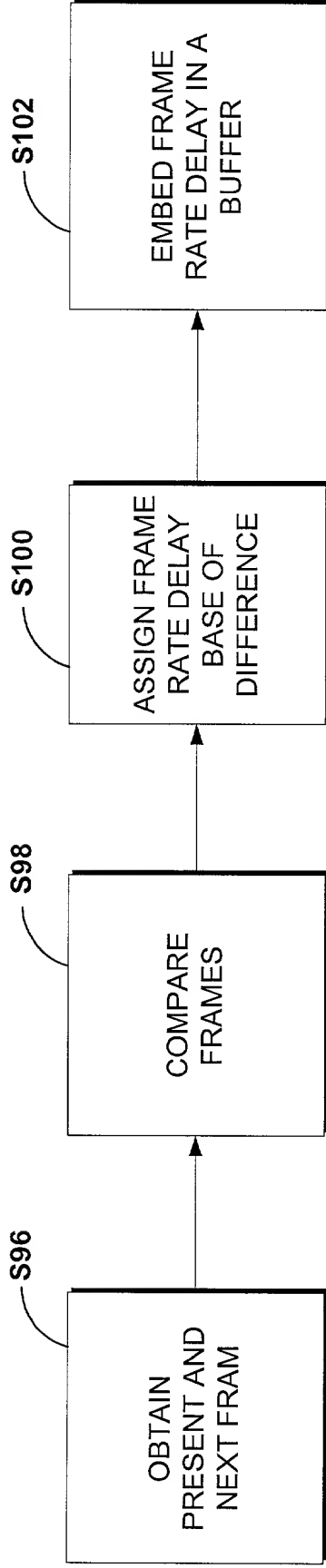


FIG. 11.

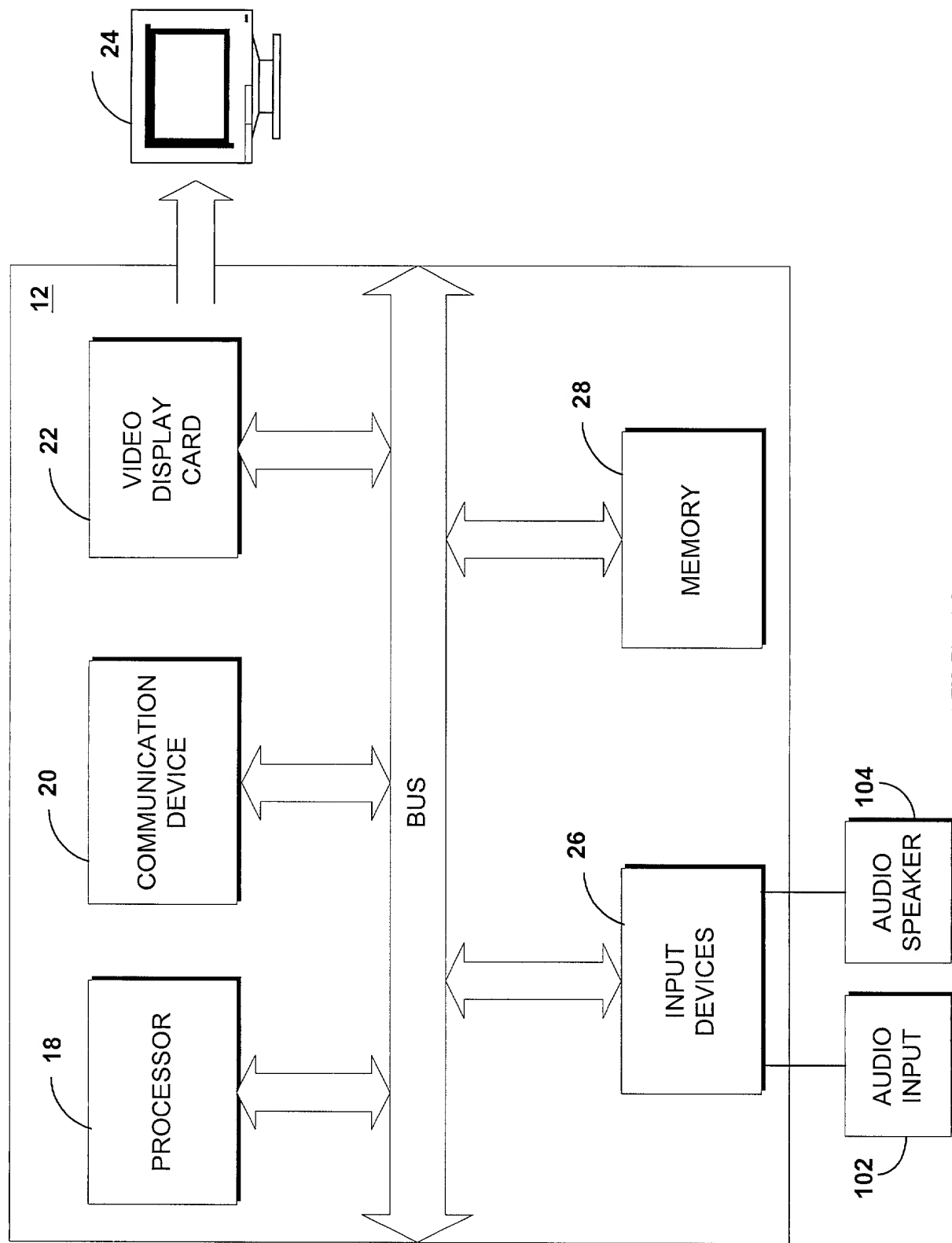


FIG. 12.